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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,339	WANG ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-14,17-23 and 26-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17,18,26 and 27* is/are allowed.

6)☒ Claim(s) *3-14,19-22,25 and 28-30* is/are rejected.

7)☐ Claim(s) _ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/28/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 8, "the hint register includes a field to specify an iteration distance" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of

the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: at page 6, line 10, "checker" should read -detector-.

Appropriate correction is required.

Claim Objections

3. Claim 9-11, 13, and 14 are objected to because of the following informalities:

In claim 9, line 5, after "iteration;", -and- should be inserted; and

In claim 13, line 2, "hint" should read -hint information- in order to consistent with the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3–14, 29, and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, line 3, "an apparatus to rotate registers in software pipelined loops" is an indefinite term since many elements such as in line 4, "a register rotation prediction unit" and in line 7, "unarchitected predicate registers" are also the "apparatus to rotate registers in software pipelined loops". Similar problems exist in the other claims 4, 5, and 9.

In claim 4, line 6, it is not clear what is meant by "the predicted register addresses are such that the buffered

instructions can be issued simultaneously with a branch instruction". Some details are missing in the language. Besides, the claim language is not proper since it forms a main sentence.

In claim 9, it is not clear why "unarchitected frame marker registers" is separately claimed as an element since the "register rotation prediction unit" (130) already contains the "unarchitected frame marker registers" (inside Frame Marker Registers 136) as shown in Fig. 1.

In claim 29, it is not clear what is meant by "a data dependence is violated" since the definition of "violate" related to the data dependence was not well defined previously. More detailed description is required.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 3-8, 12-14, 19-22, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Rau et al., "Code Generation Schema for Modulo Scheduled Loop", the 25th annual international symposium on microarchitecture, Vol: 23 (1) (2), pp 158-169, December 1992, (in the IDS mailed 3/28/01) hereafter referred to as Rau et al.

Referring to claim 3, Rau et al. discloses, as claimed, a processor comprising: an apparatus to rotate registers (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") in software pipelined loops; and a register rotation prediction unit (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164) to predict register addresses for future loop iterations (see Loop Control Operations, as shown in Sec. 2.4 on page 161); a buffer to hold buffered instructions

with predicted register addresses (this is certainly existing in the Rau et al.'s system in order to execute predicated execution as shown in Sec. 2.2 on page 161, see also Sec. 3.4 on page 164); and unarchitected predicate registers (predicate register ICR (ICP), see Sec. 2.4 on page 161, and since the values in the predicate register ICR (ICP) are invisible during the process in the Rau et al.'s system, therefore, the predicate register ICR (ICP) is interpreted as unarchitected predicate register) to predicate the buffered instructions.

Referring to claim 4, Rau et al. discloses, as claimed, a processor comprising: an apparatus to rotate registers (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") in software pipelined loops; and a register rotation prediction unit (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.2-2.4 on page 161, see also Sec. 3.4 on page 164) to predict register addresses for future loop iterations (see Loop Control Operations, as shown in Sec. 2.4 on page 161); a buffer to hold buffered instructions with predicted register addresses (this is certainly existing in

the Rau et al.'s system in order to execute predicated execution as shown in Sec. 2.2 on page 161, see also Sec. 3.4 on page 164); and the predicted register addresses are such that the buffered instructions can be issued simultaneously with a branch instruction (see Fig. 6(b), showing the at least one non branch instruction simultaneously with the at least one branch instruction in the Rau et al.'s system when speculative execution is performed).

Referring to claim 5, Rau et al. discloses, as claimed, a processor comprising: an apparatus to rotate registers (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") in software pipelined loops; and a register rotation prediction unit (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.2-2.4 on page 161, see also Sec. 3.4 on page 164) to predict register addresses for future loop iterations (see Loop Control Operations, as shown in Sec. 2.4 on page 161); and a hint register (predicate register ICR (ICP), see Sec. 2.4 on page 161, and since the values in the predicate register ICR (ICP) are used to perform speculative

(with predicting for branch instruction) execution, predicated execution, and register rotation in the Rau et al.'s system as shown in Figs. 6(b) and 10) to encode prediction hints for the register rotation prediction unit.

As to claim 6, Rau et al. also discloses: the hint register (predicate register ICR (ICP), see Sec. 2.4 on page 161, and since the values in the predicate register ICR (ICP) are used to perform speculative (with predicting for branch instruction) execution, predicated execution, and register rotation in the Rau et al.'s system as shown in Figs. 6(b) and 10) is configured to hold static hints (the initial values of the predicate register ICR (ICP)) generated by a compiler.

As to claim 7, Rau et al. also discloses: the hint register (predicate register ICR (ICP), see Sec. 2.4 on page 161, and since the values in the predicate register ICR (ICP) are used to perform speculative (with predicting for branch instruction) execution, predicated execution, and register rotation in the Rau et al.'s system as shown in Figs. 6(b) and 10) is configured to hold dynamic hints (the values of the predicate register ICR (ICP) during the process run in the Rau et al.'s system) generated at runtime.

As to claim 8, Rau et al. also discloses: the hint register (predicate register ICR (ICP), see Sec. 2.4 on page 161, and

since the values in the predicate register ICR (ICP) are used to perform speculative (with predicting for branch instruction) execution, predicated execution, and register rotation in the Rau et al.'s system as shown in Figs. 6(b) and 10) includes a field (see ICP, LC, and ESC for the loop control in Sec. 2.4, on page 161) to specify an iteration distance (see Sec. 2.4, on pages 161-162, regarding ICR (ICP) controlling the conditional execution of the next loop iteration).

Referring to claim 19, Rau et al. discloses as claimed a processing system comprising: an execution pipeline (see Sec. 1.1 on page 158, regarding software pipelining); memory (in the Rau et al.'s system, such as main memory) coupled to the execution pipeline to hold processor instructions arranged in a software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161); and register rotation prediction hardware (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations using register rotation, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164) to predict physical register values for the processor instructions in future iterations of the software loop (see Loop Control Operations using register rotation, as shown in Sec. 2.4 on page 161); a software pipeline instruction buffer (this is certainly existing

in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations using register rotation, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164 and Fig. 10(a)) coupled between the execution pipeline and the register rotation prediction hardware to hold the processor instructions in future iterations of the software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161); and the register rotation prediction hardware includes a circuit to specify complete physical register addresses (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") for the processor instructions in future iterations of the software loop.

As to claim 20, Rau et al. also discloses: processor instructions held in the software pipeline instruction buffer include fully specified physical register addresses (as set forth, see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file").

Referring to claim 21, Rau et al. discloses, as claimed, a processing system comprising: an execution pipeline (see Sec. 1.1 on page 158, regarding software pipelining); memory (in the Rau et al.'s system, such as main memory) coupled to the execution pipeline to hold processor instructions arranged in a software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161); and register rotation prediction hardware (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations using register rotation, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164) to predict physical register values for the processor instructions in future iterations of the software loop (see Loop Control Operations using register rotation, as shown in Sec. 2.4 on page 161); a software pipeline instruction buffer (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations using register rotation, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164 and Fig. 10(a)) coupled between the execution pipeline and the register rotation prediction hardware to hold the processor instructions in future iterations of the software loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161); and the register rotation prediction hardware

includes a circuit to specify complete physical register addresses (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") for the processor instructions in future iterations of the software loop; and the execution pipeline is configured to speculatively (see Sec. 2.4 on page 161, regarding the predicate register ICR (ICP) is used to perform speculative execution, predicated execution, and register rotation in the Rau et al.'s system as shown in Figs. 6(b) and 10(b)) execute instructions received from the software pipeline instruction buffer.

As to claim 22, Rau et al. also discloses: a plurality of unarchitected predicate registers (predicate register ICR (ICP), see Sec. 2.4 on page 161, and since the values in the predicate register ICR (ICP) are invisible during the process in the Rau et al.'s system, therefore, the predicate register ICR (ICP) is interpreted as unarchitected predicate register), wherein the instructions within the software pipeline instruction buffer are predicated (see Sec. 2.4 on page 161, regarding the predicate register ICR (ICP) is used to perform speculative execution, predicated execution, and register rotation in the Rau et al.'s

system as shown in Figs. 6(b) and 10(b)) on at least one of the plurality of unarchitected predicate registers.

Referring to claim 25, Rau et al. discloses, as claimed, a method of executing a software pipelined loop comprising: rotating registers (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") for each iteration of the loop (see Loop Control Operations, as shown in Sec. 2.4 on page 161); predicting (this step is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164) register rotations for future iterations of the loop; the software pipelined loop comprises at least one branch instruction (see Figs. 7 and 8 regarding at least one branch instruction in the software pipelined loop), the method further comprising issuing at least one non-branch instruction simultaneously with the at least one branch instruction (see Figs. 6(b), 7 and 8, showing the at least one non branch instruction simultaneously with the at least one branch instruction in the Rau et al.'s system); and the at least one non-branch instruction is predicated (see Sec.

2.4 on page 161, regarding the predicate register ICR (ICP) is used to perform speculative execution, predicated execution, and register rotation in the Rau et al.'s system as shown in Figs. 6(b) and 10(b)) on an unarchitected predicate register (predicate register ICR (ICP), see Sec. 2.4 on page 161, and since the values in the predicate register ICR (ICP) are invisible during the process in the Rau et al.'s system, therefore, the predicate register ICR (ICP) is interpreted as unarchitected predicate register).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 9-11, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rau et al. in view of Fite et al. (U.S. Patent No. 5,142,634) hereafter referred to as Fite et al.'634.

Referring to claim 9, Rau et al. discloses, as claimed, a processor comprising: an apparatus to rotate registers (see page 161, section 2.1, regarding "a rotating register file is addresses by adding the instruction's register specification field to the contents of the Iteration Control Pointer (ICP) modulo the number of registers in the rotating register file") in software pipelined loops; and a register rotation prediction unit (this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations, as shown in Secs. 2.2-2.4 on page 161, see also Sec. 3.4 on page 164) to predict register addresses for future loop iterations (see Loop Control Operations, as shown in Sec. 2.4 on page 161).

However, Rau et al. does not explicitly discloses: a plurality of unarchitected frame marker registers (in claim 9); speculation decision making hardware to compute values for the plurality of unarchitected frame marker registers (in claim 10); register renaming hardware in a pipeline, the register renaming hardware being responsive to the plurality of unarchitected

frame marker registers (in claim 11); and modifying at least one unarchitected frame marker register (in claim 28).

Fite et al.'634 discloses a system comprising a plurality of unarchitected frame marker registers (93, see Fig. 4, and since the marker register 93 is related to the access of the computer target address, see Col. 17, lines 49-53); speculation decision making hardware (combinational logic 91, see Fig. 4) to compute values for the plurality of unarchitected frame marker registers; and modifying at least one unarchitected frame marker register (93, see Fig. 4, and since the marker register 93 is related to the access of the computer target address, see Col. 17, lines 49-53).

Note Rau et al. also teaches to use register renaming hardware in a pipeline (note this is certainly existing in the Rau et al.'s system in order to execute predicated and speculative executions and Loop Control Operations using register rotation, as shown in Secs. 2.1-2.4 on page 161, see also Sec. 3.4 on page 164); and Fite et al.'634 discloses a system comprising a plurality of unarchitected frame marker registers (93, see Fig. 4, and since the marker register 93 is related to the access of the computer target address, see Col. 17, lines 49-53) as set forth.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Rau et al.'s system to comprise a plurality of unarchitected frame marker registers; speculation decision making hardware to compute values for the plurality of unarchitected frame marker registers; register renaming hardware in a pipeline, the register renaming hardware being responsive to the plurality of unarchitected frame marker registers; and modifying at least one unarchitected frame marker register, as taught by Fite et al.'634, in order to determining what to do with the computer target address received from the operating unit (see Col. 17, lines 49-53) to facilitate the branch prediction in a loop operation of the Rau et al.'s system.

10. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rau et al. in view of D'Sa et al. (U.S. Patent No. 6,151,671) hereafter referred to as D'Sa et al.'671.

Rau et al. discloses the claimed invention except for: a trace cache; the trace being configured to hold a prediction hint for each trace; and a trace cache fill unit to apply register rotation prediction to traces as traces are constructed.

D'Sa et al.'671 discloses a system comprising: a trace cache (TC 130, see Fig. 1b); the trace being configured to hold a prediction hint for each trace (see Col. 6, lines 49-61, regarding trace cache 130 storing the branch prediction); and a trace cache fill unit (see Col. 6, lines 49-53, regarding instruction fetch unit 110 is acting as the instruction source while trace cache unit 130 is in "build mode") to apply register rotation prediction to traces as traces are constructed.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Rau et al.'s system to comprise a trace cache; the trace being configured to hold a prediction hint for each trace; and a trace cache fill unit to apply register rotation prediction to traces as traces are constructed, as taught by D'Sa et al.'671, in order to facilitate the branch prediction (see Col. 6, lines 59-63) and speculative execution by taking advantage of the locality of reference for the Rau et al.'s system.

Allowable Subject Matter

11. Claims 17, 18, 26, and 27 are allowed.

12. Claims 29 and 30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: Rau et al. and Fite et al.'634, the closest references, and the other prior art do not teach or fairly suggest: at least one unarchitected frame marker register coupled to the register rotation prediction hardware to hold predicted register offsets for future iterations (in claim 17); speculatively removing stop bits from the at least one branch instruction (in claim 27) in combination with all of the other limitations of the respective claims. Further, the combination is not obvious.

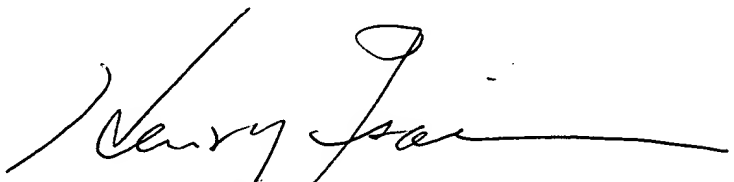
Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sager et al.'084 and Pinedo et al. also disclose the marker register shown in Fig. 3a and Fig. 2 respectively.

Contact Information

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

16. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER
November 17, 2004